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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,180	12/05/2003	Setho Sing Fee	2269-4738.2US (00-1113.02	8592

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,180	FEE ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on August 02, 2004 has been entered.

2. Claims 1-20 are presented for examination.

Double Patenting

3. Claims 1-20 of this application conflict with claims 18-35 of Application No. 09/933297. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

4. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

5. Claims 1-20 provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 18-35 of copending Application No. 09/933,297. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Regarding claim 1, Fee et al. (09/933,297) disclose: an integrated circuit package comprising: a semiconductor die; a plurality of conductive elements arranged in an array, the array including at least a first set of spaced and electrically isolated conductive elements adjacent an outer lateral periphery of the integrated circuit package and at least one other set of spaced and electrically isolated conductive elements inwardly adjacent the first set, the at least two sets of conductive elements being located outside a lateral periphery of the semiconductor die; an dielectric encapsulant formed over the semiconductor die and defining the outer lateral periphery of the integrated circuit package, the dielectric encapsulant extending at least partially laterally about the conductive elements and leaving an outer surface of each conductive element exposed; and a recess in the encapsulant material between at least one conductive element of the first set of conductive elements and at least one adjacent conductive element of the at least one other set of conductive elements. (Claim 18)

Regarding claim 2, Fee et al. (09/933,297) disclose wherein the semiconductor die includes a plurality of bond pads and wherein each of the plurality of bond pads are electrically connected with a conductive element of the plurality of conductive elements (Claim 19).

Regarding claim 3, Fee et al. (09/933,297) disclose wherein the electrical connection between each of the plurality of bond pads and each respective conductive element of the plurality of conductive elements includes a wire bond (Claim 20).

Regarding claim 4, Fee et al. (09/933,297) disclose wherein the conductive elements of the first set of conductive elements are substantially aligned with the conductive elements of the at one other set transverse to an adjacent outer lateral peripheral edge of the integrated circuit package (Claim 21).

Regarding claim 5, Fee et al. (09/933,297) disclose wherein the conductive elements of the first set of conductive elements are offset relative to the conductive elements of the at one other set (Claim 22).

Regarding claim 6, Fee et al. (09/933,297) disclose wherein the recess comprises an elongated, trough-like recess extending substantially between conductive elements of the first set and conductive elements of the second set disposed along a common laterally outer peripheral edge of the integrated circuit package (Claim 23).

Regarding claims 7, 19-20, Fee et al. (09/933,297) disclose a semiconductor die assembly, comprising: a semiconductor die having a plurality of bond pads; a lead frame having a plurality of conductive leads, each lead being electrically coupled at spaced locations on the lead to at least two bond pads of the plurality of bond pads (Claim 24).

Regarding claim 8, Fee et al. (09/933,297) disclose further comprising a dielectric encapsulant formed about the semiconductor die and partially about the lead frame (Claim 25).

Regarding claim 9, Fee et al. (09/933,297) disclose further comprising a wire bond coupling each lead at the spaced locations thereon to one of the at least two

bond pads of the plurality of bond pads (Claim 26).

Regarding claim 10, Fee et al. (09/933,297) disclose wherein each lead includes a severance region configured to facilitate separation into at least two mutually electrically isolated conductive elements (Claim 27).

Regarding claim 11, Fee et al. (09/933,297) disclose : a module board configured to be electrically coupled with a higher level of packaging; and at least one integrated circuit package electrically coupled with the module board, the integrated circuit package comprising: a semiconductor die; a plurality of conductive elements arranged in an array, the array including at least a first set of spaced and electrically isolated conductive elements adjacent an outer lateral periphery of the integrated circuit package and at least one other set of spaced and electrically isolated conductive elements inwardly adjacent the first set, the at least two sets of conductive elements being located outside a lateral periphery of the semiconductor die; an dielectric encapsulant formed over the semiconductor die and defining the outer lateral periphery of the integrated circuit package, the dielectric encapsulant extending at least partially laterally about the conductive elements and leaving an outer surface of each conductive element exposed; and a recess in the encapsulant material between at least one conductive element of the first set of conductive elements and at least one adjacent conductive element of the at least one other set of conductive elements (Claim 28).

Regarding claim 12, Fee et al. (09/933,297) disclose a computer system comprising: an input device; an output device; a processor coupled to the input and

output devices; and a memory module coupled to the processor, the memory module comprising a module board coupled to at least one integrated circuit packagecomprising: a semiconductor die; a plurality of conductive elements arranged in an array, the array including at least a first set of spaced and electrically isolated conductive elements adjacent an outer lateral periphery of the integrated circuit package and at least one other set of spaced and electrically isolated conductive elements inwardly adjacent the first set, the at least two sets of conductive elements being located outside a lateral periphery of the semiconductor die; an dielectric encapsulant formed over the semiconductor die and defining the outer lateral periphery of the integrated circuit package, the dielectric encapsulant extending at least partially laterally about the conductive elements and leaving an outer surface of each conductive element exposed; and a recess in the encapsulant material between at least one conductive element of the first set of conductive elements and at least one adjacent conductive element of the at least one other set of conductive elements (Claim 29).

Regarding claim 13, Fee et al. (09/933,297) disclose a semiconductor die assembly, comprising: a semiconductor die having a plurality of bond pads on an active surface thereof; at least one set of mutually spaced conductive elements laterally outboard of at least one peripheral edge of the semiconductor die, and at least another set of mutually spaced conductive elements spaced from and laterally outboard of the at least one set of conductive elements; a plurality of wire bonds

extending between bond pads of the plurality and conductive elements of the first and second sets; and a package comprising dielectric material extending over the semiconductor die and wire bonds and having an outer lateral periphery substantially coincident with outer lateral extents of the at least one other set of conductive elements, dielectric material of the package extending at least partially about each of the conductive elements and leaving a surface thereof exposed (Claim 30).

Regarding claim 14, Fee et al. (09/933,297) disclose further comprising a die paddle to which the semiconductor die is secured by a back side thereof (Claim 31).

Regarding claim 15, Fee et al. (09/933,297) disclose wherein the at least one set of mutually spaced conductive elements and the at least another set of conductive elements extend around a plurality of peripheral edges of the semiconductor die (Claim 32).

Regarding claim 16, Fee et al. (09/933,297) wherein the at least one set of mutually spaced conductive elements and the at least another set of conductive elements extend around four peripheral edges of the semiconductor die (Claim 33).

Regarding claim 17, Fee et al. (09/933,297) disclose further including an elongated, trough-like recess extending between conductive elements of the at least one set and conductive elements of the at least another set and substantially parallel to the at least one peripheral edge of the semiconductor die (Claim 34).

Regarding claim 18, Fee et al. (09/933,297) disclose wherein the exposed surfaces of the conductive elements are oriented substantially parallel to the active surface of the semiconductor die (Claim 35).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER